

<b>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</b>	
In re application of: <b>Bruce B. Doris et al.</b>	Date: <b>April 20, 2007</b>
Serial Number: <b>10/604,190</b>	Examiner: <b>Tu Tu V. Ho</b>
Filed: <b>06/30/2003</b>	Group Art Unit: <b>2818</b> Confirmation No.: <b>1189</b>
Title: <b>HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE</b>	IBM Corporation D/18G, B/321, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

**LETTER TO OFFICIAL DRAFTSPERSON**

Commissioner of Patents and Trademarks  
Alexandria, VA 22313

Dear Sir:

Responsive to the Examiner's comment #3, attached is a replacement Drawing sheet showing a corrected Figure 3(b).

Corrected Figure 3(b) clarifies width "transistor region R" described in paragraph 34 of the specification as filed.

Further, element 80 as shown in Figure 3(b) is a tensile barrier etch stop layer 80 described, e.g., in paragraph 33 of the specification as filed.

Respectfully submitted,  
Bruce B. Doris et al.

By:

*[Signature]* *20 Apr. 2007*  
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